gate insulating film **103**, the gate electrode **105**, the source electrode **106**, the drain electrode **107**, etc. may be formed as in the case of the MISFET having the inverted channel structure. While the example of forming the first insulating film **131** after the second insulating film **132** was shown in FIG. **20**, the first insulating film **131** may be formed before the second insulating film **132**. In the case of the stored channel structure, also, wet etching may be performed after formation of the second insulating film **132**, and a top portion of the trench **102***a* may be rounded. Also, a p-type MISFET may be formed.

[0094] Furthermore, not only the MISFETs, but various types of semiconductor devices that have an electrode placed on a semiconductor layer via an insulating film can be fabricated in a similar manner. For example, an insulated gate bipolar transistor (IGBT) can be formed by imparting different conductivity types to the substrate and the semiconductor layer directly formed thereon.

[0095] While the example of a plurality of unit cells arranged in a zigzag fashion was described in this embodiment, the unit cells may be arranged in any fashion. Also, while the example of the trench having a square planar shape was described, the trench may have any planar shape. For example, the trench may have a rectangular planar shape, and the unit cells may be arranged so that the major sides of a plurality of trenches extend in parallel with each other.

[0096] In this embodiment, the example of the substrate **101** being made of 4H—SiC and the semiconductor layer **102** being formed on the (0001) Si plane was described. Alternatively, the semiconductor layer **102** may be formed on a (000-1) C plane and the drain electrode **107** may be formed on the (0001) Si plane. Otherwise, the plane direction of the principal surface may be of another crystal plane. Further, another polytype SiC substrate may be used.

[0097] While the semiconductor device using SiC was described in this embodiment, the present disclosure is also applicable to a semiconductor device using another wide band-gap semiconductor such as gallium nitride (GaN) and diamond. Also, the present disclosure is applicable to a semiconductor device using silicon.

INDUSTRIAL APPLICABILITY

[0098] The semiconductor device and the fabrication method for the same of the present disclosure are useful as various types of semiconductor devices including power devices and fabrication methods for the same.

DESCRIPTION OF REFERENCE CHARACTERS

[0099] **11** Unit Cell
[0100] **101** Substrate
[0101] **102** Semiconductor Layer
[0102] **102***a* Trench
[0103] **103** Gate Insulating Film
[0104] **105** Gate Electrode
[0105] **105**A Conductive Film
[0106] **106** Source Electrode
[0107] **107** Drain Electrode
[0108] **121** Drift Region
[0109] **123** Body Region
[0110] **124** Source Region
[0111] **125** Channel Layer
[0112] **131** First Insulating Film
[0113] **132** Second Insulating Film
[0114] **132**A Inner-Trench Portion
[0115] **132**B Trench-Periphery Portion
[0116] **141** Resist Layer

1. A fabrication method for a semiconductor device, comprising the steps of:
- preparing a substrate having a semiconductor layer provided on a principal surface;
- forming a trench in the semiconductor layer;
- forming a gate insulating film on a side of the trench, a bottom of the trench, and a periphery of the trench; and
- forming a conductive film on the gate insulating film to fill the trench and extend on the periphery of the trench,
- wherein
- the step of forming a gate insulating film includes a step of forming a first insulating film on the side of the trench and a step of forming a second insulating film on the bottom of the trench and the periphery of the trench using a high-density plasma chemical vapor deposition method, the thickness of portions of the gate insulating film formed on the bottom of the trench and the periphery of the trench being made larger than that of a portion of the gate insulating film formed on the side of the trench, and
- in the step of forming a conductive film, the conductive film is formed to be in contact with a portion of the first insulating film formed on the side of the trench.

2. The fabrication method for a semiconductor device of claim **1**, wherein
- the step of forming a first insulating film is performed after the step of forming a second insulating film.

3. The fabrication method for a semiconductor device of claim **1**, wherein
- the step of forming a first insulating film is performed before the step of forming a second insulating film.

4. The fabrication method for a semiconductor device of claim **1**, wherein
- the step of forming a trench includes a step of rounding a top end portion of the trench.

5. The fabrication method for a semiconductor device of claim **1**, further comprising the step of:
- wet-etching the second insulating film before the step of forming a conductive film,
- wherein
- the etching amount of the second insulating film is 30% or less of the thickness of the second insulating film.

6. The fabrication method for a semiconductor device of claim **1**, wherein
- in the step of preparing a substrate, the semiconductor layer is formed to have a drift region of a first conductivity type and a body region of a second conductivity type provided on the drift region,
- in the step of forming a trench, the trench is formed so that the bottom thereof is located below an interface between the drift region and the body region and above the bottom of the drift region, and
- in the step of forming a gate insulating film, the gate insulating film is formed so that the top surface of the portion thereof formed on the bottom of the trench is located below the interface between the drift region and the body region.

7. The fabrication method for a semiconductor device of claim **1**, wherein
- the semiconductor layer is made of a wide band-gap semiconductor.